**STIMULATION AND CHARACTERIZATION OF NANO SCALED FET**

**Submitted**

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**(Duration: 22/07/2024 to 19/03/2025)**



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**DECLARATION**

**I/We declare that the project work contained in this report is original and it has been done by me under the guidance of my project guide.**

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**CERTIFICATE**

**This is to certify that Niharika Sidda,Pasupuleti Sushanth,Jillela Mounika bearing BU21EECE0100374,BU21EECE0100466,BU21EECE0100448 has satisfactorily completed Capstone Project Entitled in partial fulfillment of the requirements as prescribed by University for VIIIth semester, Bachelor of Technology in “Electrical, Electronics and Communication Engineering” and submitted this report during the academic year 2024-2025.**

**[Signature of the Guide] [Signature of HOD]**

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# **Chapter 1: Introduction:**

Nanoscaled Field-Effect Transistors (FETs) are tiny electronic components used in modern devices like smartphones and computers. As technology advances, these FETs are becoming smaller and more complex, making their behavior harder to predict and understand,also reaching the nanometer scale (less than 100 nm). However, making these tiny transistors work efficiently is challenging due to issues like leakage current,short-channel effects, and power dissipation. To solve these problems, we are trying to test and study different types of Field Effect Transistors (FETs) and test their performance using simulation and characterization techniques.To address this,we use simulation and characterization techniques to make it easier.

* **Simulation**: We used TCAD (Technology Computer-Aided Design) software to predict how FETs will behave before manufacturing.
* If the simulation results show any problems, the design can be modified before manufacturing, saving time and cost,like
* How much current flows through the transistor?
* How much power does it consume?
* Does it heat up too much?
* **Characterization**: Involves real-world testing of FETs to measure their electrical, structural, and thermal performance.
* **Electrical performance**: How efficiently does it switch on and off?
* **Thermal behavior**: Does it overheat during operation?

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## **1.1 Overview of the problem statement:**

"To analyze and compare the performance of DGIMFET, IM-FET, JL-FET, and DGJL-FET using simulation and characterization techniques, identifying their advantages, limitations, and suitability for advanced semiconductor applications."

## **1.2 Objectives and goals:**

* Simulate nanoscale FETs (DGIM-FET, IM-FET, JL-FET, DGJL-FET) using TCAD tools to predict their behavior.
* Compare their performance in terms of current control, leakage, power efficiency, and scalability.
* Identify the best FET design for different applications based on simulation and real-world data.

**Main Goals**

* Performance Optimization
* Understanding Behavior
* Scaling Down Further
* Exploring New Materials

**GITHUB links:**

| **Parameter** | **IM-FET** | **DGIM-FET** | **JL-FET** | **nDGJL-FET** |
| --- | --- | --- | --- | --- |
| **Size** | Moderate | Smaller than IMFET | Very Small | Smallest among all |
| **Speed** | Moderate | Fast | Fast but slower than DGIM | Fastest |
| **Thermal Stability** | Moderate | Better than IMFET | lower stability | Best |
| **Majority Carriers** | Electrons (n-type) / Holes (p-type) | Electrons (n-type) / Holes (p-type) | Electrons (n-type) / Holes (p-type) | Electrons (n-type) / Holes (p-type) |
| **Minority Carriers** | Few due to inversion layer | Fewer than IMFET | Not Available(no junction) | Almost negligible |

| **Parameter** | **IM - FET** | **DGIM-FET** | **JL-FET** | **nDGJL-FET** |
| --- | --- | --- | --- | --- |
| **Leakage Current** | High | Low | Low | Very Low |
| **Threshold Voltage (Vth)** | Moderate | Lower than IMFET | Lowest among all | Optimal (better than JL but controlled) |
| **ID vs VG Plot** | Standard like MOSFET | Steeper than IMFET | Slower rise | Steepest increase |
| **Doping Profile** | Normal doping | High doping in channel region | Uniform doping throughout | Ultra-thin uniform doping |
| **Fabrication Complexity** | Standard CMOS | More complex due to double-gate | Easier than DGIM but has leakage issues | Most complex but best performance |

| **Parameter** | **IM-FET** | **DGIM-FET** | **JL-FET** | **nDGJL-FET** |
| --- | --- | --- | --- | --- |
| **power consumption** | High | Moderate | Low | Lowest |
| **scalability** | Low | Medium | High | Very high |
| **Heat Dissipation** | High | Medium | Low | Lowest |
| **Applications** | General MOSFET applications | High-speed and low-power applications | Low-power but high-leakage applications | Ultra-low power, high-performance applications |

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# **Chapter 2 : Literature Review:**

| **TITLE** | **AUTHOR** | **YEAR** | **TECHNOLOGY USED** | **SUMMARY** | **PRO** | **LIMITATION** |
| --- | --- | --- | --- | --- | --- | --- |
| Device and circuit performance analysis of double gate junctionless transistors at Lg = 18 nm | Chitrakant Sahu,  Jawar Singh | 2014 | ATLAS TCAD mixed-mode simulator | JL DG devices outperform IM FETs with better speed and stability. | Faster performance and improved SRAM stability | JL design complexity compared to conventional CMOS. |
| Analysis of Delta-Doped and Uniformly Doped AlGaAs/GaAs HEMTs by Ensemble Monte Carlo Simulations | Ki Wook Kim, Hong Tian, Michael A. Littlejohn | 1991 | Uniformly doped AlGaAs/GaAs high electron mobility transistors (HEMTs) | Delta-doped HEMTs outperform uniform ones in electron density and speed. | Improved transconductance and drain current drive | Increased complexity in device structure and fabrication. |

| **TITLE** | **AUTHOR** | **YEAR** | **TECHNOLOGY USED** | **SUMMARY** | **PRO** | **LIMITATION** |
| --- | --- | --- | --- | --- | --- | --- |
| A Physics-Based Threshold Voltage Model for Junctionless Double Gate FETs Having Vertical Structural and Doping Asymmetry | A. Kumar,  J. N. Roy | 2019 | Synopsys Sentaurus Device simulation tool,  MATLAB | Model for asymmetric JL DG FETs simplifies analysis while maintaining accuracy | Simplifies complex calculations with improved accuracy. | May not account for all real-world device variations. |
| Impact of Single Charged Gate Oxide Defects on the Performance and Scaling of Nanoscaled FETs | J. Franco, B. Kaczer, M. Toledano-Luque, et al. | 2012 | Nanoscaled Field-Effect Transistors (FETs)  particularly pFinFETs and planar pMOSFETs, which include SiGe channel devices | NBTI reliability in nanoscaled FETs varies by technology, impacting scaling | SiGe channel devices exhibit reduced time-dependent variability, enhancing NBTI robustness. | The severe 1/area scaling rule complicates reliability predictions for further scaling. |

| **TITLE** | **AUTHOR** | **YEAR** | **TECHNOLOGY USED** | **SUMMARY** | **PRO** | **LIMITATION** |
| --- | --- | --- | --- | --- | --- | --- |
| Thermo-magnetic effects on MOSFETs simulated and experimentally characterized for reliability 5th | Gabriela A. Rodríguez-Ruiz et al. | 2015 | Thermo-magnetic modeling and simulation in nano-scaled MOSFETs. | The paper introduces a simulation method for studying the effects of temperature and magnetic fields on the gate tunneling current in MOSFET devices. | Provides a new method for mapping electronic properties in nanoscaled MOSFETs. | Simulation and experimental setup are complex and require precise control. |

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# **Chapter 3 : Strategic Analysis and Problem Definition:**

# **3.1 SWOT Analysis:**

SWOT Analysis is defined as Strengths,Weaknesses,Opportunities & Threats. Here’s the SWOT Analysis:

### **Strengths:** **Weaknesses:**

1.Precise Analysis 1.Simulation Accuracy

2.Time-Saving 2.Assumptions Approximations

3.Enhanced Optimization

**Opportunities: Threats:**

1.Technology Advancement 1.Rapid Technological Changes

2.Integration with AI/ML 2.High Competition

3.Miniaturization Trend 3.Data Security Risks

4.Cross-Disciplinary Collaboration

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# **Chapter 4 : Methodology:**

**1.Device Modelling:**

Since nanoscale transistors are extremely small, their behavior is affected by quantum mechanical effect**s** (like electron tunneling and charge confinement). To study these effects, researchers use computational models instead of directly fabricating the transistors.

**How It helps in our Project:**

* We used TCADsoftware to create virtual models of DGIM-FET, IM-FET, JL-FET, and DGJL-FET.
* These models will simulate how electrons move through the transistor and predict key properties like current flow, leakage, and power efficiency.
* The simulation will help you understand which transistor type performs better before manufacturing.

**Electrical Characterization**:

* **I-V Characteristics** : It measures how current (I) changes with voltage (V) to see how efficiently the transistor switches ON and OFF.
* **Threshold Voltage (Vth):** The minimum voltage needed to turn the transistor ON.
* **Subthreshold Slope** : Tells how quickly the transistor turns ON from an OFF state (important for power efficiency).

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### **4.1 Tools and techniques utilized:**

* **Design Specifications:** Define key parameters such as channel length, width, and material properties.Use CAD tools like TCAD.
* **Material Selection:** Choose suitable semiconductor materials (e.g., silicon, graphene, MoS2) based on desired electrical properties and scalability.
* **Current-Voltage (I-V) Testing**: Measures how much current flows through the FET at different voltages. This shows how well the FET turns on and off,like

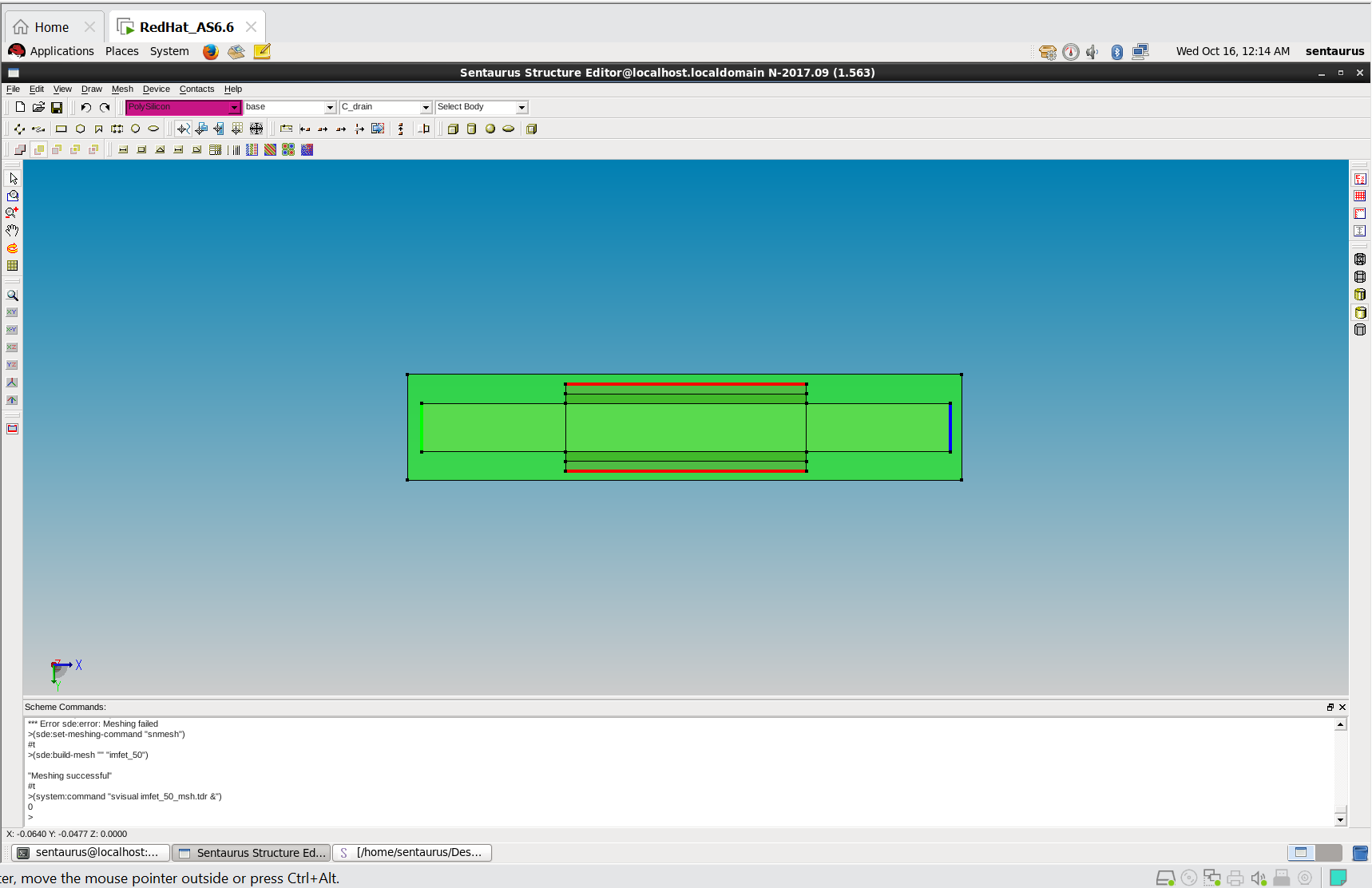
**IV Curve Tracing Techniques**:

* **Sweep Measurement**: Applying a voltage/current sweep and measuring response.
* **Pulsed I-V Measurement**: Reduces heating effects for accurate testing.
* **Logarithmic Sweeps**: Used for low-current devices like MOSFETs.

#### **4.3 Design considerations:**

* **Scaling and Size**: As transistors get smaller, controlling short-channel effects like leakage current and Drain-Induced Barrier Lowering becomes more difficult. Proper scaling is essential to maintain efficiency.
* **Material Selection**: Using advanced materials, such as high-k dielectrics (for gate insulation) or new semiconductors like GaN or graphene, can enhance performance by reducing leakage and improving speed.
* **Quantum Effects**: At the nanoscale, quantum mechanical effects like tunneling and electron confinement significantly impact device behavior, so they need to be considered in design.
* **Power Consumption**: Reducing power consumption is critical, especially for low-power applications. Techniques like using multi-gate architectures help reduce power while maintaining high performance.

**Chapter 5 : Implementation:**



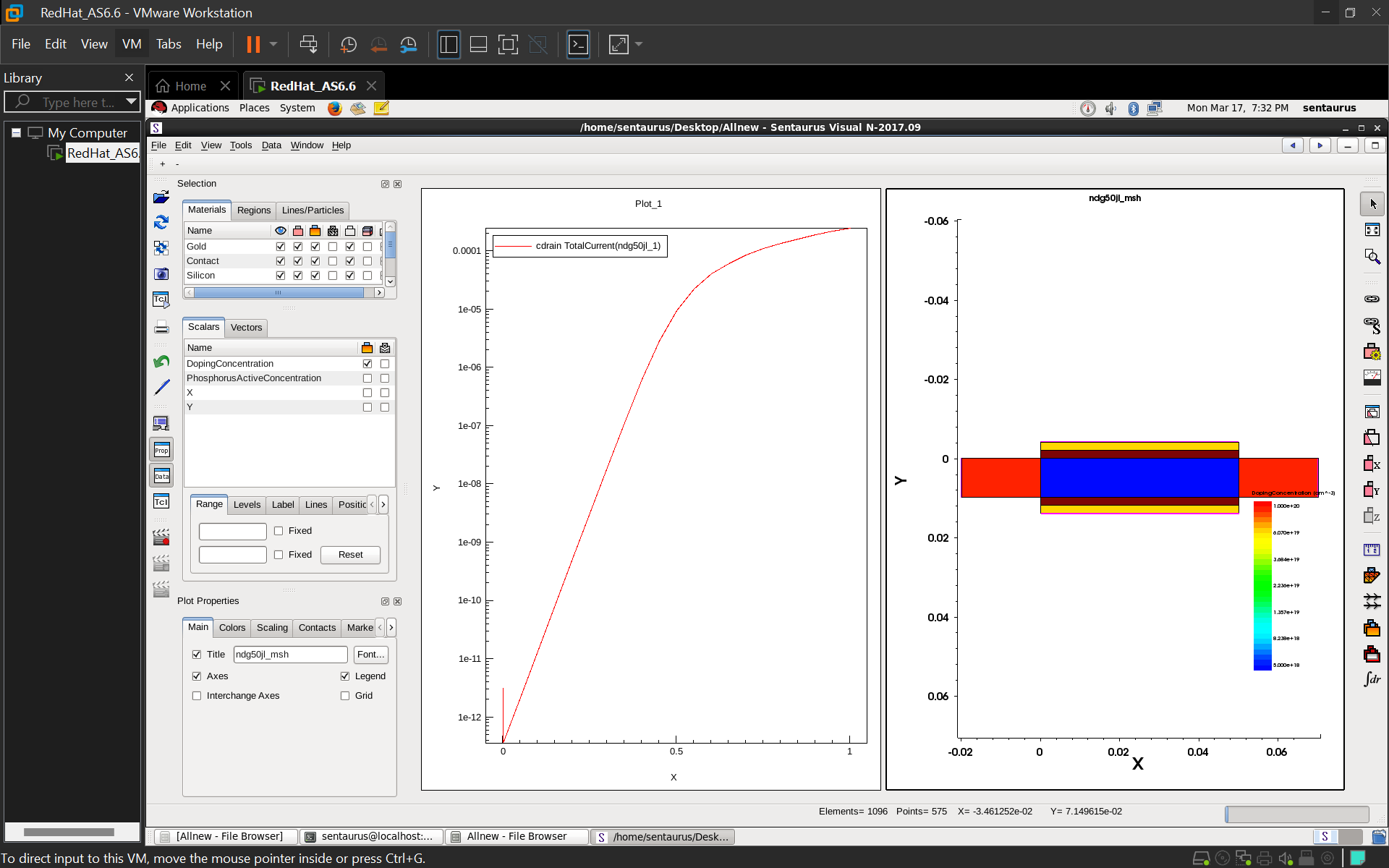
## **5.1 Description of how the project was executed**

The image shows a TCAD Sentaurus Structure Editor interface, used to design and simulate a nanoscale FET (Field-Effect Transistor). The structure is created by defining **materials, doping regions, and device contacts**. Here's how it is implemented:

1. **Device Creation**:
   * The substrate (green region) represents the semiconductor (e.g., silicon).
   * The red and blue lines indicate different layers, likely gate, source, and drain.
2. **Meshing Process**:
   * A simulation grid (mesh) is applied to divide the structure into small elements for solving equations.
   * The error message suggests an initial meshing failure, but later it was successfully generated.
3. **Simulation Preparation**:
   * After meshing, the device undergoes electrical simulations like I-V characteristics, capacitance, and leakage current analysis.
   * It helps study transistor behavior under different voltages.

This is the common structure of all the types of MOSFETs that we are going to study and compare.

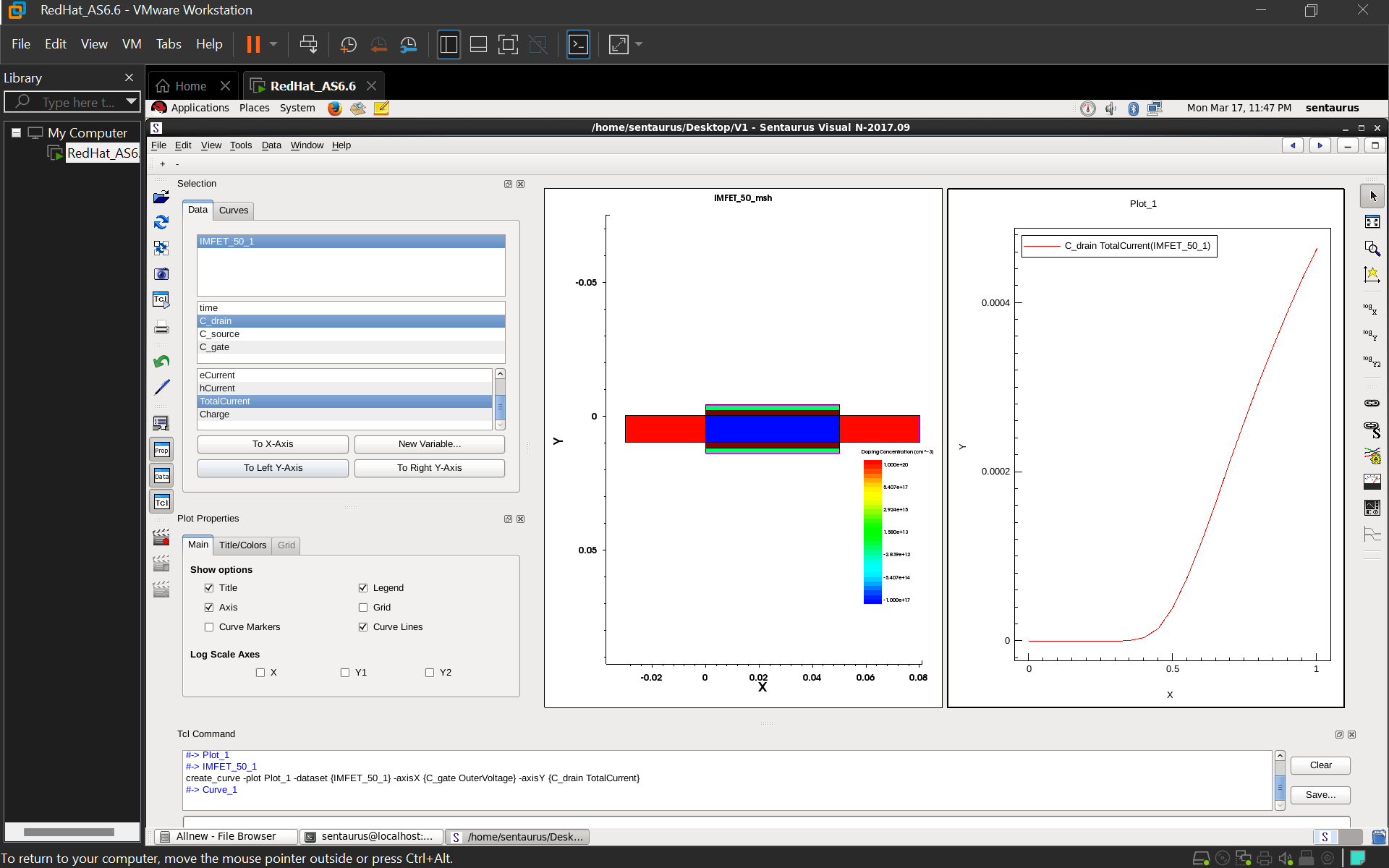
**1.nDGJLFET:**



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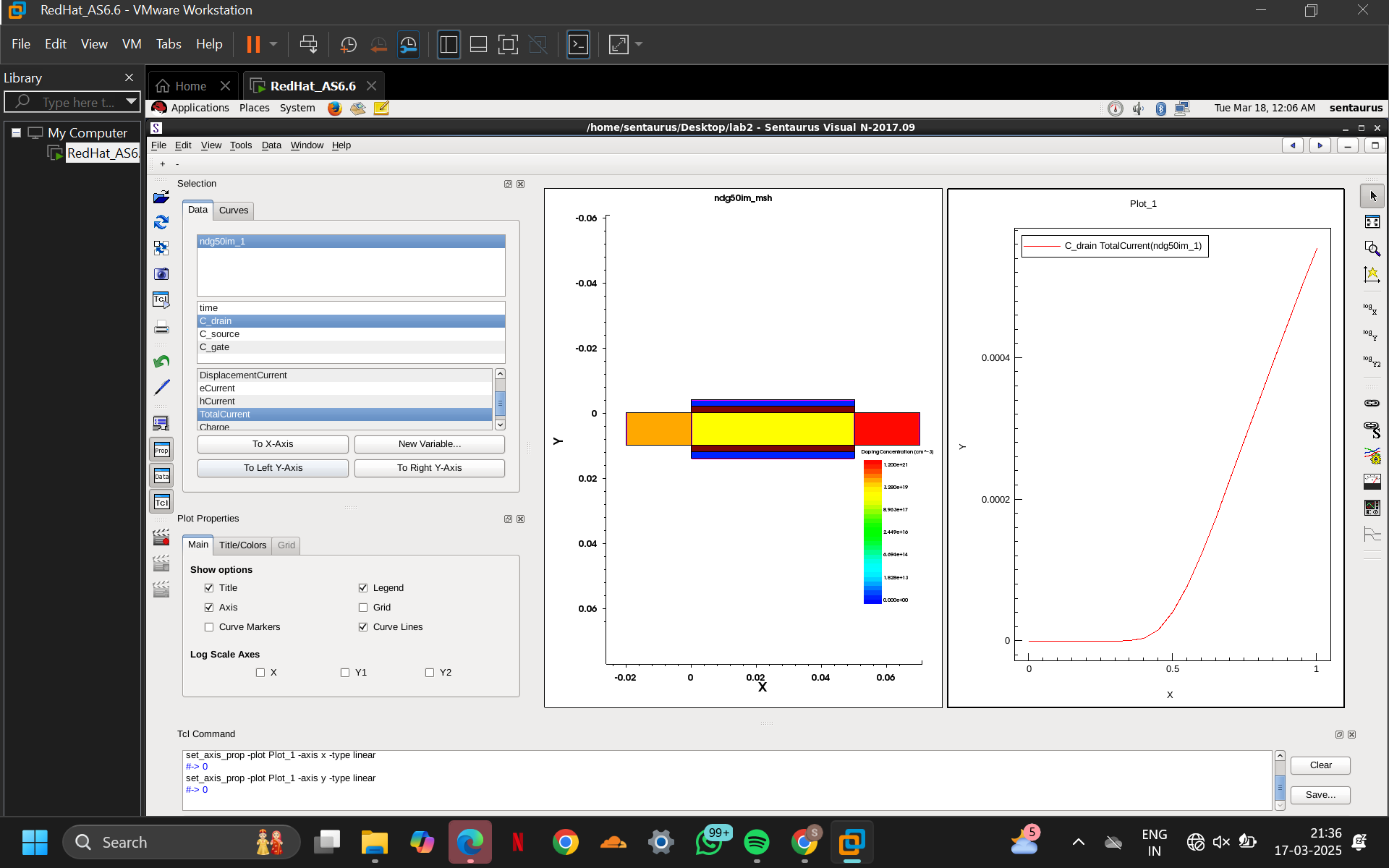
* The above picture is the structure and plot of an n-type double gate junctionless FET of 50 nm channel length(nDGJL50) . Here,
* Blue colored region - Channel(doping conc - 5 x 10^18) also it is the lowest doping concentration.
* Red colored region- Source,drain(doping conc - 1x10^20) highest doping concentration.
* Yellow is the metal region where we used gold.
* Brown represents the metal oxide.
* The graph is between gate voltage and drain current and it increases as the voltage increases.

**2.IMFET\_50**



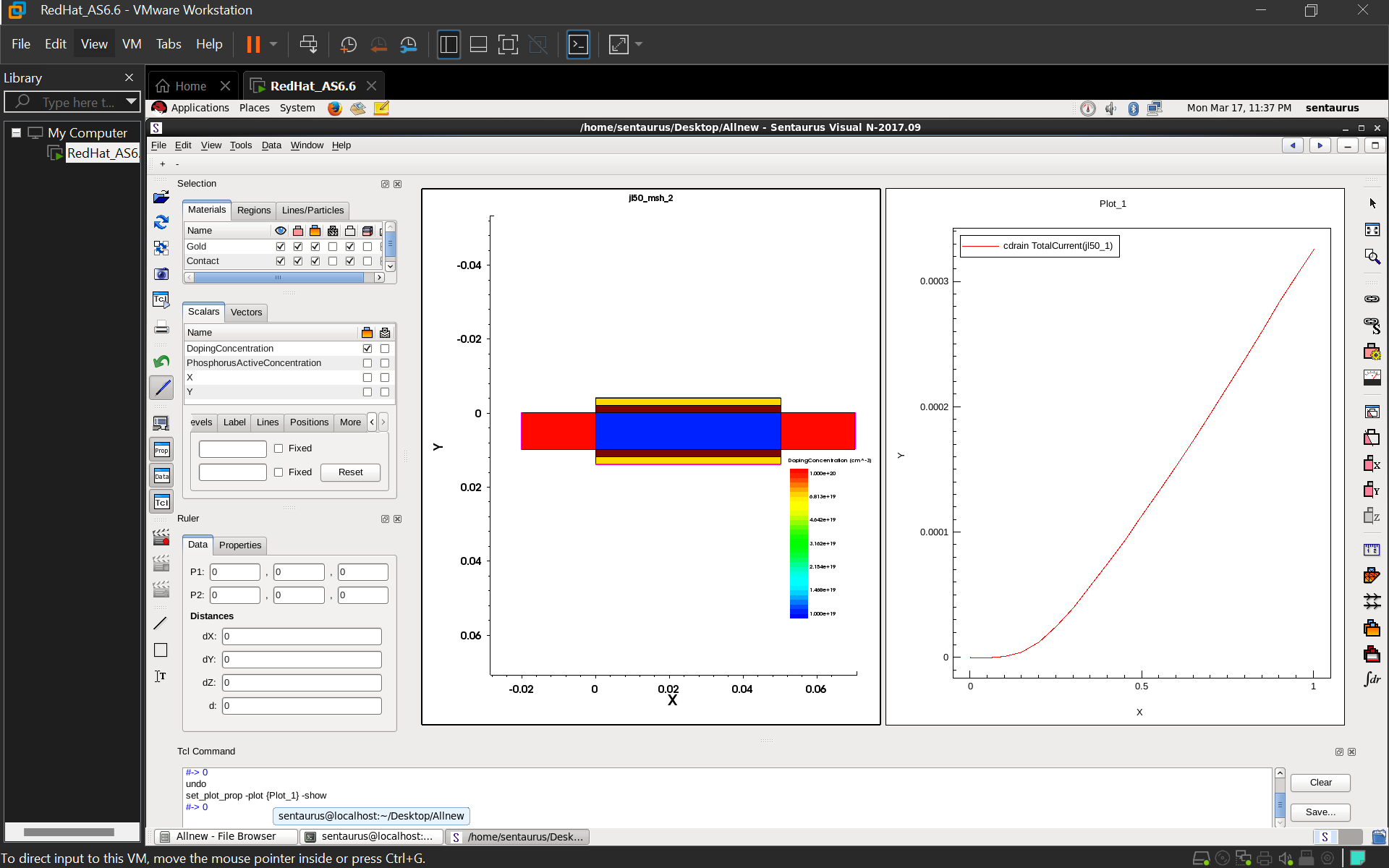
* The above picture is the structure and plot of an IMFET(inversion mode) of 50 nm channel length(nDGJL50) . Here,
* Blue colored region - Channel(doping conc - 5 x 10^17) also it is the lowest doping concentration.
* Red colored region- Source,drain(doping conc - 1x10^20) highest doping concentration.
* Green is the metal region where we used polysilicon.
* Brown represents the metal oxide(SiO2).
* The graph is between gate voltage and drain current and it increases as the voltage increases.

**3. DGIM50:**

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* The above picture is the structure and plot of a double gate inversion mode FET of 50 nm channel length(nDGIM50) . Here,
* Yellow colored region - Channel(doping conc - 5 x 10^17) also it is the lowest doping concentration.
* Red ,Orange colored region- Source,drain(doping conc - 1x10^20) highest doping concentration.
* Yellow is the metal region where we used gold.
* Blue represents the metal oxide.
* The graph is between gate voltage and drain current and it increases as the voltage increases.

**4.JL50:**

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* The above picture is the structure and plot of a junctionless FET of 50 nm channel length(JL50) . Here,
* Blue colored region - Channel(doping conc - 1 x 10^19) also it is the lowest doping concentration.
* Red colored region- Source,drain(doping conc - 1x10^20) highest doping concentration.
* Yellow is the metal region where we used gold.
* Brown represents the metal oxide.
* The graph is between gate voltage and drain current and it increases as the voltage increases.

**Chapter 6:Results**

| **Name** | **IM-FET** | **DGIM-FET** | **JL-FET** | **nDGJL-FET** |
| --- | --- | --- | --- | --- |
| **Threshold Voltage** | 0.474346V | 0.472654V | 0.27251V | 0.5539V |
| **GmMax** | 0.000950 | 0.00110 | 0.0004529 | 0.00055 |
| **Ioff(Id at Vg=0)** | 2.49 x 10^ -18 A | 1.75 x 10^ - 19 A | 5.28 x 10 ^ -17 A | 3.17 x 10^-12 A |
| **Id sat** | 0.000465 A | 0.000555 A | 0.000326 A | 0.000246 A |
| **R out** | 1.839 x 10 ^ 6 | 1.655 x 10 ^ 6 | 2.130 x 10 ^ 6 | 2.054 x 10 ^ 6 |
| **R On** | 0 | 0 | 0 | 0 |

Based on all the given parameters, **DGIM-FET is the best choice** for your project. Here's why:

**1.Best Performance (GmMax = 0.00110)**

* + Higher **GmMax** means better amplification and switching speed.
  + DGIM-FET has the highest value, making it the most efficient.

**2.Lowest Power Consumption (Ioff = 1.75 × 10⁻¹⁹ A)**

* + It has the **lowest leakage current**, meaning less power is wasted when the device is off.

**3.Highest Drive Strength (Id,sat = 0.000555 A)**

* + It provides the **highest saturation current**, which means it can handle more load and perform better.

**4.Balanced Output Resistance (Rout = 1.655 × 10⁶ Ω)**

* + Good output resistance ensures stable operation and less power loss.

**5.Versatile Applications:**

* Can be used in both analog and digital circuits due to its balance of speed and power.
* Ideal for VLSI circuits, IoT devices, and low-power processors.

# **Chapter 7: Conclusion:**

In this project, we analyzed four types of FETs (IM-FET, DGIM-FET, JL-FET, and nDGJL-FET) based on key parameters like threshold voltage, transconductance, leakage current, saturation current, and output resistance.

After comparing all factors, DGIM-FET emerges as the best choice due to its superior performance and efficiency. It has the highest transconductance (GmMax) for better signal amplification, the lowest leakage current (Ioff) for minimal power loss, and the highest saturation current (Id,sat) for strong drive capability. Additionally, its balanced output resistance ensures stable operation. While other FETs have their advantages, DGIM-FET provides the best combination of speed, efficiency, and power handling, making it ideal for VLSI applications. Therefore, DGIM-FET is the most suitable choice.

# **Chapter 8 : Challenges & Future Work:**

**Challenges :**

**1.Comparing with Other FETs:**

* To prove NDGIMFET\_50 is better, you must simulate and compare other devices.
* This increases workload and needs extra validation.

**2.Optimization Issues**:

* Finding the best doping concentration and material properties can be tricky.
* Small changes can affect threshold voltage (Vth) and current flow.

**3**.**Material Properties:**

* Any small variation in doping or gate material can change results.
* Requires careful calibration with real-world data.

**4. Mesh Optimization:**

* A fine mesh is needed for accurate results, finding the right balance is tricky.

**5.Long Simulation Time:**

* Simulation using TCAD generally takes a long time, so we have to be extra careful while performing simulations.
* Even a minor error can lead to building of the structure from the initial stage.

**Future Work** :

**1.Optimize Mesh for Faster Simulation:**

* Improve mesh refinement techniques to balance accuracy and speed.
* Use adaptive meshing to reduce unnecessary computation.

**2.Enhance Material Models:**

* Implement advanced material properties for better accuracy.
* Explore new gate and channel materials for improved performance.

**3.Exploring New Materials :**

* Investigate 2D materials (like graphene, MoS₂) or high-k dielectrics to enhance transistor efficiency.

**4.Compare with Experimental Data:**

* Validate the simulation by comparing it with real fabricated devices.
* Adjust parameters to match experimental results.

**5.Expand to 3D Simulation:**

* Move from 2D to 3D modeling for more realistic results.
* Study how short-channel effects behave in 3D.

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